IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An IC chip for reading an image, comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors;

a plurality of dummy photoelectric conversion elements, each of which is arranged ~~respectively near~~ in close proximity to and forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements, and is shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors; and

an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal,

wherein the output circuit outputs a difference between the first ~~and second~~ photoelectric conversion ~~signals~~ signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, so as to correct the first photoelectric conversion signal.

2-3. (Canceled).

4. (Currently Amended) An IC chip for reading an image, comprising:

a plurality of first processing sections, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors; and

a first signal output line by way of which the first photoelectric conversion signal is transmitted;

a plurality of second processing sections provided so as to pair respectively with the first processing sections, the second processing sections each comprising:

a plurality of dummy photoelectric conversion elements, each of which is arranged ~~respectively near~~ in close proximity to and forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements, and is shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors; and

a second signal output line by way of which the second photoelectric conversion signal is transmitted;

an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal; and

a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit,

wherein the output circuit outputs a difference between the first ~~and second~~ photoelectric conversion ~~signals~~ signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, so as to correct the first photoelectric conversion signal.

5. (Currently Amended) An image reading device comprising:

one or more IC chips, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors;

a plurality of dummy photoelectric conversion elements, each of which is arranged ~~respectively near~~ in close proximity to and forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements, and is shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors;

an output circuit for outputting a difference between the first ~~and second~~ photoelectric conversion ~~signals~~ signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, as a corrected first photoelectric conversion signal;

a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage;

a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage;

a clock input terminal by way of which a clock is fed in; and

a reference voltage input terminal by way of which a reference voltage for the output circuit is fed in; and

an A/D converter for converting a signal output from the output circuit into a digital signal,

wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

6-7. (Canceled).

8. (Currently Amended) An image reading device comprising:

one or more IC chips, each comprising:

a plurality of first processing sections, each comprising:

a plurality of image reading photoelectric conversion elements;

a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements;

a first signal selection circuit for sequentially selecting the plurality of first transistors; and

a first signal output line by way of which the first photoelectric conversion signal is transmitted;

a plurality of second processing sections provided so as to pair respectively with the first processing sections, the second processing sections each comprising:

a plurality of dummy photoelectric conversion elements, each of which is arranged ~~respectively near~~ in close proximity to and forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements, and is shielded from light;

a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements;

a second signal selection circuit for sequentially selecting the plurality of second transistors; and

a second signal output line by way of which the second photoelectric conversion signal is transmitted;

an output circuit for outputting a difference between the first ~~and second~~ photoelectric conversion ~~signals~~ signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, as a corrected first photoelectric conversion signal;

a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit;

a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage;

a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage; and

a clock input terminal by way of which a clock is fed in;

an A/D converter for converting a signal output from the output circuit into a digital signal,

wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.